In the Claims:

Please cancel claims 1-8 and 15-22. Please cancel claim 13. Please amend claims 9-12 and 14. Please add new claims 23-37. The claims are as follows.

9. (Currently amended) A method for forming a ~~field effect transistor~~ semiconductor device, the method comprising the steps of:

a) providing a semiconductor substrate;

b) patterning the semiconductor substrate to provide a body, the body having a first side and a second side;

c) forming a first double gate, the first double gate having a first portion adjacent to the body first side and a second portion adjacent to said body second side;

d) forming a second double gate, the second double gate having a first portion adjacent to the body first side and a second portion adjacent to the said body second side, the first portion of the first double gate having a surface that is coplanar with a surface of the first portion of the second double gate, the second portion of the first double gate having a surface that is coplanar with a surface of the second portion of the second double gate.

10. (Currently amended) The method of claim 9, wherein the step of patterning the semiconductor substrate to provide a body comprises patterning the semiconductor substrate to form a fin type body.

11. (Currently amended) The method of claim 9, wherein the semiconductor substrate comprise a silicon-on-insulator layer and wherein the step of patterning the semiconductor substrate to provide a body comprises patterning the silicon-on-insulator layer.

12. (Currently amended) The method of claim 9, further comprising the step of forming an insulating spacer between the first double gate and the second double gate.

13. (Canceled)

14. (Currently amended) The method of claim 9, further comprising the steps of forming a contact on the first double gate to provide a first control signal and a contact on the second double gate to provide a second control signal.

23. (New) The method of claim 9, wherein the body comprises a fin type body, and wherein the fin type body has a width narrow enough to insure a fully depleted channel during operation of the semiconductor device.

24. (New) The method device of claim 9, wherein the first side of the body and the second side of the body are on opposite sides of the body.

25. (New) The method device of claim 9, wherein the first double gate is adapted to receive a first control signal and the second double gate is adapted to receive a second control signal.

26. (New) A method for forming a semiconductor device, the method comprising the steps of:

a) providing a semiconductor substrate;

b) patterning the semiconductor substrate to provide a body, the body having a first side and a second side;

c) forming a first double gate, the first double gate having a first portion adjacent to the body first side and a second portion adjacent to said body second side;

d) forming a second double gate, the second double gate having a first portion adjacent to the body first side and a second portion adjacent to the said body second side, wherein the step of forming an insulating spacer between the first double gate and the second double gate comprises forming a first insulating spacer between the first portion of the first double gate and the first portion of the second double gate, and forming a second insulating spacer between the second portion of the first double gate and the second portion of the second double gate.

27. (New) The method of claim 26, wherein the first insulating spacer and second insulating spacer are formed offset such that the first insulating spacer and second insulating spacer are not inline across the body.

28. (New) The method of claim 26, wherein the body comprises a fin type body, and wherein the fin type body has a width narrow enough to insure a fully depleted channel during operation of the semiconductor device.

29. (New) The method of claim 26, wherein the first side of the body and the second side of the body are on opposite sides of the body.

30. (New) A method for forming a transistor, comprising:

a) forming a fin body on a substrate, the fin body having a first vertical edge and a second vertical edge, and a first end and a second end;

b) forming a source at the first end of the fin body, and forming a drain at the second end of the fin body;

c) forming a first gate structure adjacent the transistor body first vertical edge and second vertical edge, the first gate structure approximate to the source;

d) forming a second gate structure adjacent the transistor body first vertical edge and second vertical edge, the second gate structure approximate to the drain.

31. (New) The method of claim 30, further comprising forming a spacer between the first gate structure and the second gate structure, wherein the portion of the spacer adjacent to the first vertical edge is offset from the portion of the spacer adjacent to the second vertical edge.

32. (New) The method of claim 30, wherein a portion of the first gate structure adjacent to the first vertical edge of the transistor body is directly opposite a portion of the second gate structure adjacent to the second vertical edge of the transistor body.

33. (New) The method of claim 32, wherein the first gate structure adjacent to the first vertical

edge off the transistor body has a work function which is more attractive to dominant charge carriers of the transistor compared to that of the first gate structure adjacent to the second vertical edge of the transistor body.

34. (New) The method of claim 33, wherein the second gate structure adjacent to the second vertical edge of the transistor body has a work function which is more attractive to the dominant charge carriers of the transistor compared to that of the second gate structure adjacent to the first vertical edge of the transistor body.

35. (New) The method of claim 30, wherein an edge of the first gate structure adjacent to the first vertical edge of the transistor body is opposite, and displaced less than the body thickness from an edge of the second gate structure adjacent to the second vertical edge of the transistor body.

36. (New) The method of claim 35, wherein the fin body has a width narrow enough to insure a fully depleted channel during operation of the transistor.

37. (New) The method of claim 35, wherein the first side of the fin body and the second side of the fin body are on opposite sides of the fin body.